

FSB50325

Smart Power Module (SPM®)

Features

- 250V 3.0A 3-phase FRFET inverter including high voltage integrated circuit (HVIC)
- 3 divided negative dc-link terminals for inverter current sensing applications
- HVIC for gate driving and undervoltage protection
- 3/5V CMOS/TTL compatible, active-high interface
- Optimized for low electromagnetic interference
- · Isolation voltage rating of 1500Vrms for 1min.



General Description

FSB50325 is a tiny smart power module (SPM®) based on FRFET technology as a compact inverter solution for small power motor drive applications such as fan motors and water suppliers. It is composed of 6 fast-recovery MOSFET (FRFET), and 3 half-bridge HVICs for FRFET gate driving. FSB50325 provides low electromagnetic interference (EMI) characteristics with optimized switching speed. Moreover, since it employs FRFET as a power switch, it has much better ruggedness and larger safe operation area (SOA) than that of an IGBT-based power module or one-chip solution. The package is optimized for the thermal performance and compactness for the use in the built-in motor application and any other application where the assembly space is concerned. FSB50325 is the most solution for the compact inverter providing the energy efficiency, compactness, and low electromagnetic interference.



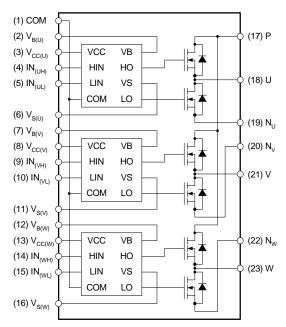


Absolute Maximum Ratings

Symbol	Parameter	Conditions	Rating	Units
V _{PN}	DC Link Input Voltage, Drain-source Voltage of each FRFET		250	V
I _{D25}	Each FRFET Drain Current, Continuous	T _C = 25°C	1.5	Α
I _{D80}	Each FRFET Drain Current, Continuous	T _C = 80°C	1.0	Α
I _{DP}	Each FRFET Drain Current, Peak	T _C = 25°C, PW < 100μs	3.0	Α
P _D	Maximum Power Dissipation	T _C = 80°C, Each FRFET	4.5	W
V _{CC}	Control Supply Voltage Applied between V _{CC} and COM		20	V
V _{BS}	High-side Bias Voltage	Applied between V _B and V _S	20	V
V _{IN}	Input Signal Voltage	Applied between IN and COM	-0.3 ~ VCC+0.3	V
TJ	Operating Junction Temperature		-20 ~ 150	°C
T _{STG}	Storage Temperature		-50 ~ 150	°C
$R_{ heta JC}$	Junction to Case Thermal Resistance	Each FRFET under inverter operating condition (Note 1)	10.2	°C/W
V _{ISO}	Isolation Voltage	60Hz, Sinusoidal, 1 minute, Connection pins to heatsink	1500	V _{rms}

Pin Descriptions

Pin Number	Pin Name	Pin Description	
1	СОМ	IC Common Supply Ground	
2	V _{B(U)}	Bias Voltage for U Phase High Side FRFET Driving	
3	V _{CC(U)}	Bias Voltage for U Phase IC and Low Side FRFET Driving	
4	IN _(UH)	Signal Input for U Phase High-side	
5	IN _(UL)	Signal Input for U Phase Low-side	
6	V _{S(U)}	Bias Voltage Ground for U Phase High Side FRFET Driving	
7	V _{B(V)}	Bias Voltage for V Phase High Side FRFET Driving	
8	V _{CC(V)}	Bias Voltage for V Phase IC and Low Side FRFET Driving	
9	IN _(VH)	Signal Input for V Phase High-side	
10	IN _(VL)	Signal Input for V Phase Low-side	
11	V _{S(V)}	Bias Voltage Ground for V Phase High Side FRFET Driving	
12	V _{B(W)}	Bias Voltage for W Phase High Side FRFET Driving	
13	V _{CC(W)}	Bias Voltage for W Phase IC and Low Side FRFET Driving	
14	IN _(WH)	Signal Input for W Phase High-side	
15	IN _(WL)	Signal Input for W Phase Low-side	
16	V _{S(W)}	Bias Voltage Ground for W Phase High Side FRFET Driving	
17	Р	Positive DC-Link Input	
18	U	Output for U Phase	
19	N _U	Negative DC-Link Input for U Phase	
20	N _V	Negative DC–Link Input for V Phase	
21	V	Output for V Phase	
22	N _W	Negative DC-Link Input for W Phase	
23	W	Output for W Phase	



Note:

Source terminal of each MOSFET is not connected to supply ground or bias voltage ground inside SPM[®]. External connections should be made as indicated in Figure 2 and 5.

Figure 1. Pin Configuration and Internal Block Diagram (Bottom View)

$\textbf{Electrical Characteristics} \ \, (\text{T}_{\text{J}} = 25^{\circ}\text{C}, \, \text{V}_{\text{CC}} = \text{V}_{\text{BS}} = 15 \text{V Unless Otherwise Specified})$

Inverter Part (Each FRFET Unless Otherwise Specified)

Symbol	Parameter	Conditions		Тур	Max	Units
BV _{DSS}	Drain-Source Breakdown Voltage	V_{IN} = 0V, I_D = 250 μ A (Note 2)	250	-	-	V
$\Delta BV_{DSS}/$ ΔT_{J}	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, Referenced to 25°C	-	0.31	-	V
I _{DSS}	Zero Gate Voltage Drain Current	V _{IN} = 0V, V _{DS} = 250V	-	-	250	μΑ
R _{DS(on)}	Static Drain-Source On-Resistance	V _{CC} = V _{BS} = 15V, V _{IN} = 5V, I _D = 1.0A		1.4	1.8	Ω
V_{SD}	Drain-Source Diode Forward Voltage	V _{CC} = V _{BS} = 15V, V _{IN} = 0V, I _D = -1.0A		-	1.2	V
t _{ON}		V _{PN} = 150V, V _{CC} = V _{BS} = 15V, I _D = 1.0A		1076	-	ns
t _{OFF}		$V_{IN} = 0V \leftrightarrow 5V, R_{EH} = 0\Omega$	-	660		ns
t _{rr}	Switching Times	Inductive load L=3mH High- and low-side FRFET switching	-	108	-	ns
E _{ON}		Tright and low side that LT switching		47	-	μЈ
E _{OFF}		(Note 3)	-	3.1	-	μJ
RBSOA	Reverse-bias Safe Operating Area	$\begin{array}{l} \text{Der-} & \text{V}_{\text{PN}} = 200\text{V}, \text{V}_{\text{CC}} = \text{V}_{\text{BS}} = 15\text{V}, \text{I}_{\text{D}} = \text{I}_{\text{DP}}, \text{R}_{\text{EH}} = 0\Omega \\ \text{V}_{\text{DS}} = \text{BV}_{\text{DSS}}, \text{T}_{\text{J}} = 150^{\circ}\text{C} \\ \text{High- and low-side FRFET switching (Note 4)} \end{array}$		Full	Square	

Control Part (Each HVIC Unless Otherwise Specified)

Symbol	Parameter	Conditions		Min	Тур	Max	Units
I _{QCC}	Quiescent V _{CC} Current	V _{CC} =15V, V _{IN} =0V	Applied between V _{CC} and COM	-	-	160	μΑ
I _{QBS}	Quiescent V _{BS} Current	V _{BS} =15V, V _{IN} =0V	Applied between V _B and V _S	-	-	100	μΑ
UV _{CCD}	Low-side Undervoltage	V _{CC} Undervoltage I	Protection Detection Level	7.4	8.0	9.4	V
UV _{CCR}	Protection (Figure 6)	V _{CC} Undervoltage Protection Reset Level		8.0	8.9	9.8	V
UV _{BSD}	High-side Undervoltage	V _{BS} Undervoltage Protection Detection Level		7.4	8.0	9.4	V
UV _{BSR}	Protection (Figure 7)	V _{BS} Undervoltage Protection Reset Level		8.0	8.9	9.8	V
V _{IH}	ON Threshold Voltage	Logic High Level	Annella di batana an INI and COM		-	-	V
V _{IL}	OFF Threshold Voltage	Logic Low Level	Applied between IN and COM	-	-	0.8	V
I _{IH}	Input Bias Current	V _{IN} = 5V	Applied between IN and COM	-	10	20	μΑ
I _{IL}	Input bias Current	V _{IN} = 0V	Applied between in and COM	-	-	2	μΑ

Note:

Package Marking & Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FSB50325	FSB50325	SPM23AA	ı	ı	15

^{1.} For the measurement point of case temperature $\mathsf{T}_\mathsf{C},$ please refer to Figure 3 in page 4.

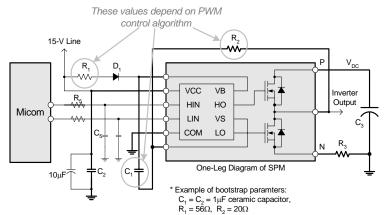
^{2.} BV_{DSS} is the absolute maximum voltage rating between drain and source terminal of each FRFET inside SPM[®]. V_{PN} should be sufficiently less than this value considering the effect of the stray inductance so that V_{DS} should not exceed BV_{DSS} in any case.

^{3.} t_{ON} and t_{OFF} include the propagation delay time of the internal drive IC. Listed values are measured at the laboratory test condition, and they can be different according to the field applications due to the effect of different printed circuit boards and wirings. Please see Figure 4 for the switching time definition with the switching test circuit of Figure 5.

^{4.} The peak current and voltage of each FRFET during the switching operation should be included in the safe operating area (SOA). Please see Figure 5 for the RBSOA test circuit that is same as the switching test circuit.

Recommended Operating Conditions

Symbol	Parameter	Conditions	Value			Units
Syllibol	raiailletei	Conditions		Тур.	Max.	Ullits
V _{PN}	Supply Voltage	Applied between P and N	-	150	200	V
V _{CC}	Control Supply Voltage	Applied between V _{CC} and COM	13.5	15	16.5	V
V_{BS}	High-side Bias Voltage	Applied between V _B and V _S	13.5	15	16.5	V
V _{IN(ON)}	Input ON Threshold Voltage	Applied between IN and COM	3.0		V _{CC}	V
V _{IN(OFF)}	Input OFF Threshold Voltage	Applied between IIV and COM	0		0.6	V
t _{dead}	Blanking Time for Preventing Arm-short	V _{CC} =V _{BS} =13.5 ~ 16.5V, T _J ≤ 150°C	1.0	-	-	μS
f _{PWM}	PWM Switching Frequency	$T_J \le 150$ °C	-	15	-	kHz
T _C	Case Temperature	$T_{J} \le 150^{\circ}C$	-20		125	°C

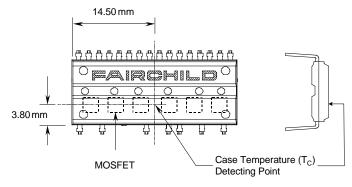


HIN	LIN	Output	Note
0	0	Z	Both FRFET Off
0	1	0	Low-side FRFET On
1	0	V _{DC}	High-side FRFET On
1	1	Forbidden	Shoot-through
Open	Open	Z	Same as (0, 0)

Note:

- (1) It is recommended the bootstrap diode D_1 to have soft and fast recovery characteristics with 600-V rating
- (2) Parameters for bootsrap circuit elements are dependent on PWM algorithm. For 15 kHz of switching frequency, typical example of parameters is shown above.
- (3) RC coupling(R₅ and C₅) at each input (indicated as dotted lines) may be used to prevent improper input signal due to surge noise. Signal input of SPM[®] is compatible with standard CMOS or LSTTL outptus.
- (4) Bold lines should be short and thick in PCB pattern to have small stray inductance of circuit, which results in the reduction of surge voltage. Bypass capacitors such as C₁, C₂ and C₃ should have good high-frequency characteristics to absorb high-frequency ripple current.

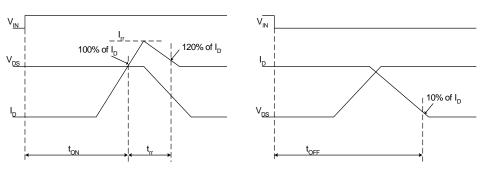
Figure 2. Recommended CPU Interface and Bootstrap Circuit with Parameters



Note:

Attach the thermocouple on top of the heatsink-side of SPM® (between SPM® and heatsink if applied) to get the correct temperature measurement.

Figure 3. Case Temperature Measurement



(a) Turn-on (b) Turn-off Figure 4. Switching Time Definition

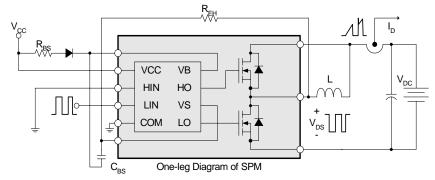


Figure 5. Switching and RBSOA(Single-pulse) Test Circuit (Low-side)

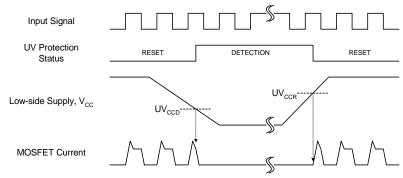


Figure 6. Undervoltage Protection (Low-side)

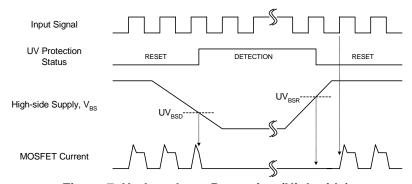


Figure 7. Undervoltage Protection (High-side)

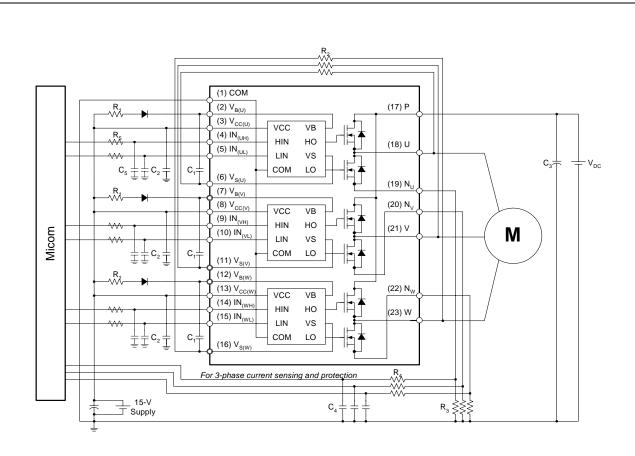
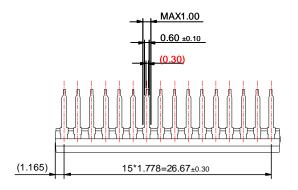
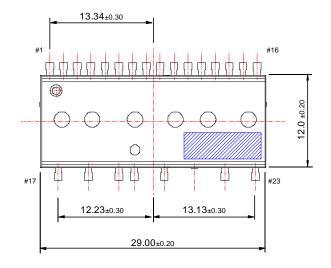
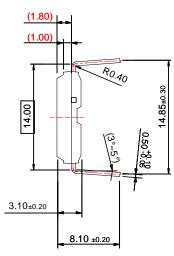


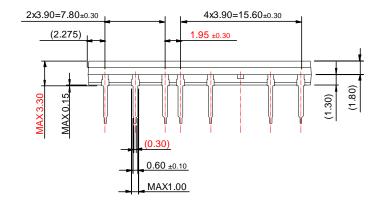
Figure 8. Example of Application Circuit

Detailed Package Outline Drawings













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